

This diagram shows a cross-sectional view of a semiconductor device along the X-Z plane. The device is divided into three main regions: two 'SIDE REGION C' areas on the left and right, and a 'CENTRAL REGION D' in the middle. The total width of the device is labeled 'G1'. The width of the central region is labeled 'Tw'. The width of each side region is labeled '30a'. The central region is further divided into sub-regions '30b' and '30a'. The device consists of several layers: a top layer (43), a layer with a central opening (42), a layer with a central opening (41), a layer with a central opening (40), a layer with a central opening (38), a layer with a central opening (34a), a layer with a central opening (33), a layer with a central opening (32), a layer with a central opening (31), a layer with a central opening (23), a layer with a central opening (34), and a bottom layer (20). A dashed line 'A' indicates a specific feature or interface. A coordinate system is shown in the top right corner with X, Y, and Z axes.

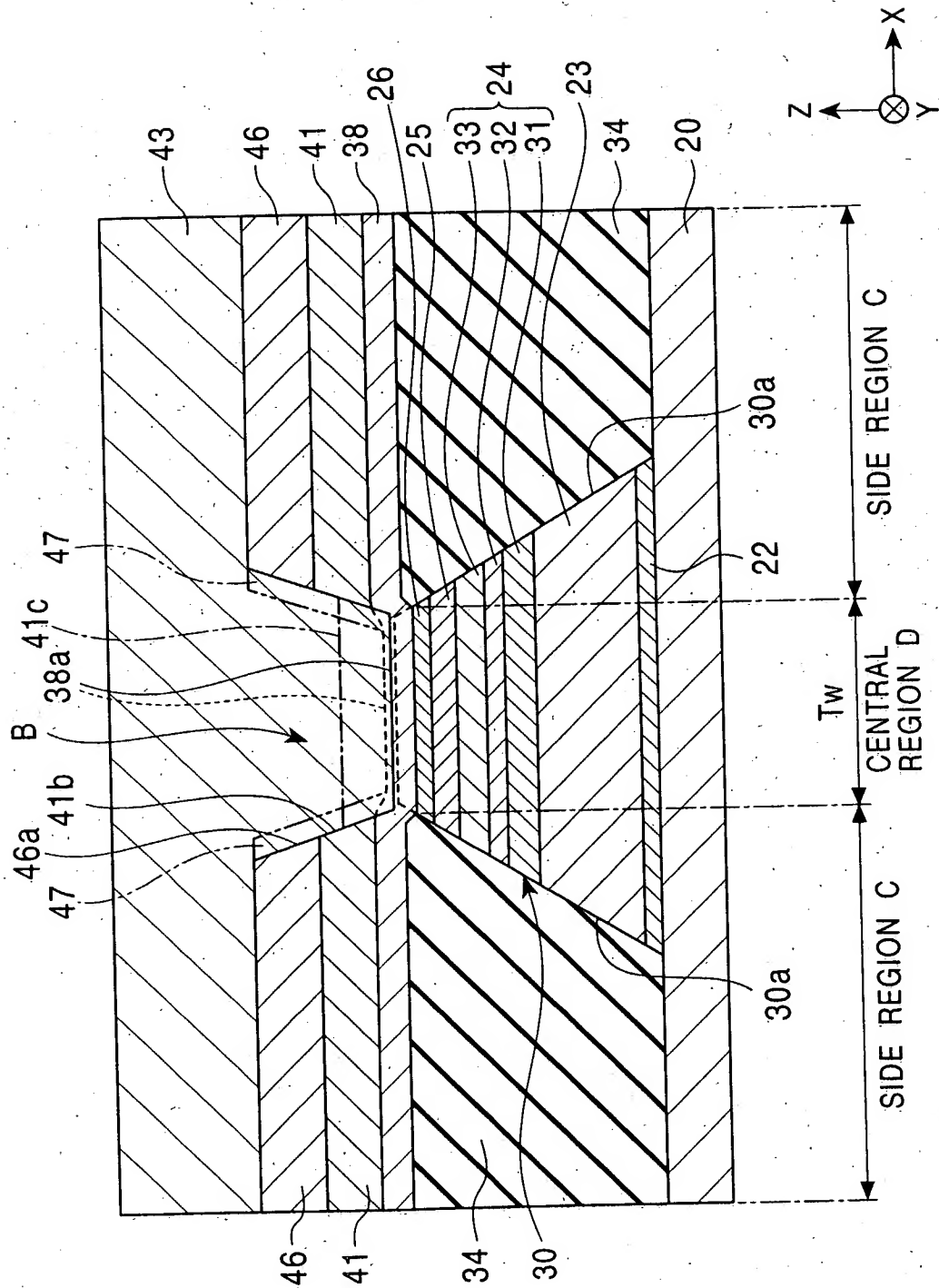
Diagram illustrating a cross-sectional view of a semiconductor device structure, showing a central region D and two side regions C.

The structure includes a substrate 20, a gate stack 22, and a channel layer 23. A central region D is defined by a width T_w , and two side regions C are defined by a width $30a$. The device is divided into three regions: 24, 25, and 26. A dashed line 27 indicates a boundary. A coordinate system (X, Y, Z) is shown in the top right corner.

Labels and components shown in the diagram include:

- Regions: 24, 25, 26
- Widths: $30a$, T_w
- Structural layers: 20, 22, 23, 24, 25, 26, 27, 30, 31, 32, 33, 34, 38, 41, 42, 43, 44
- Coordinate system: X, Y, Z

FIG. 3



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FIG. 4

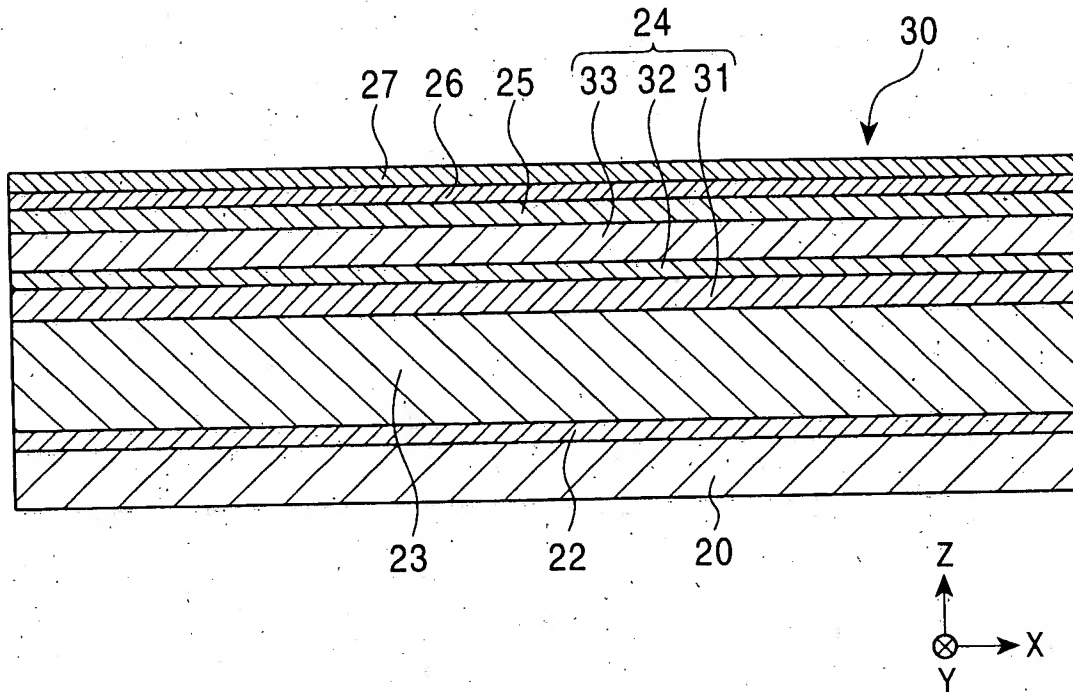
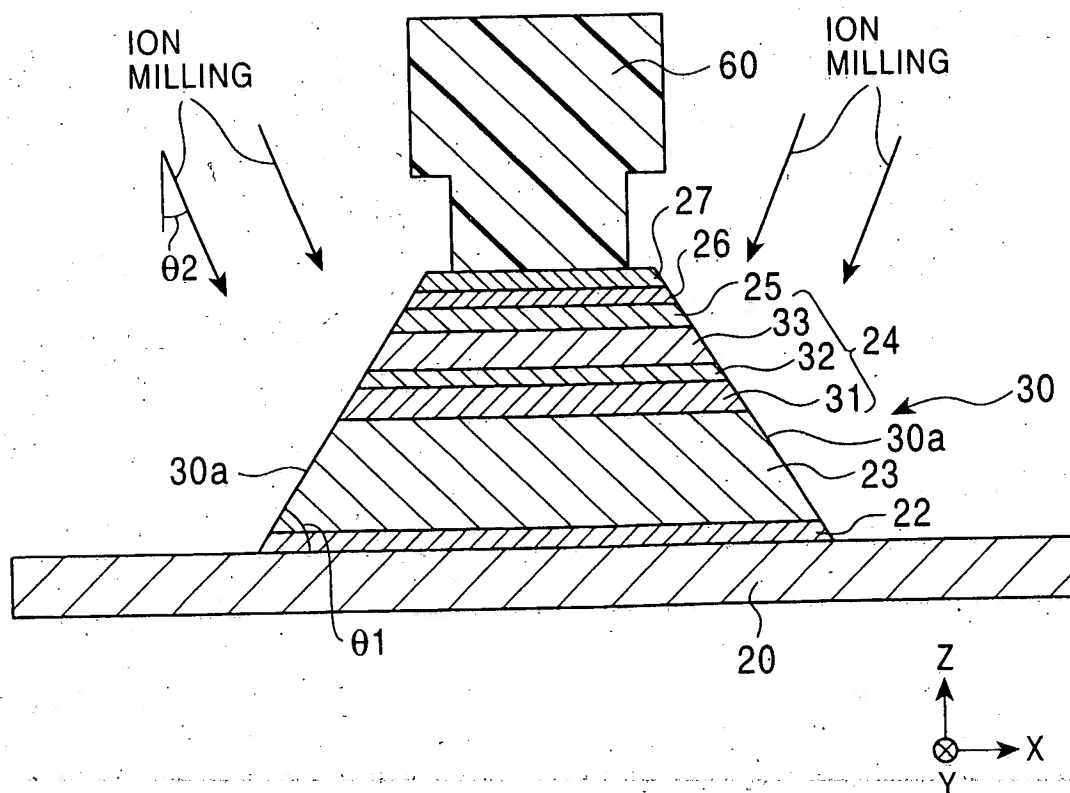


FIG. 5



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FIG. 6

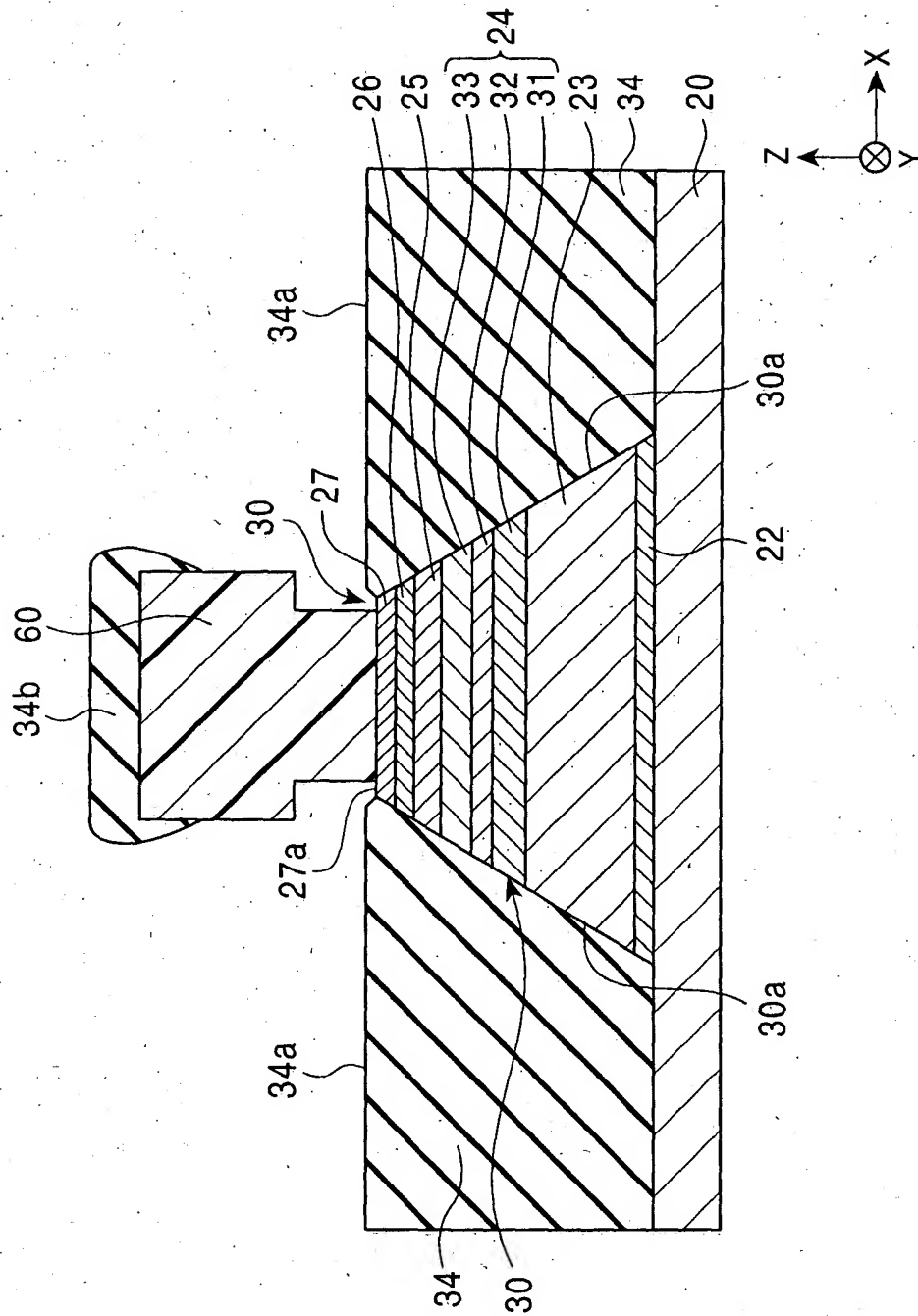


FIG. 7

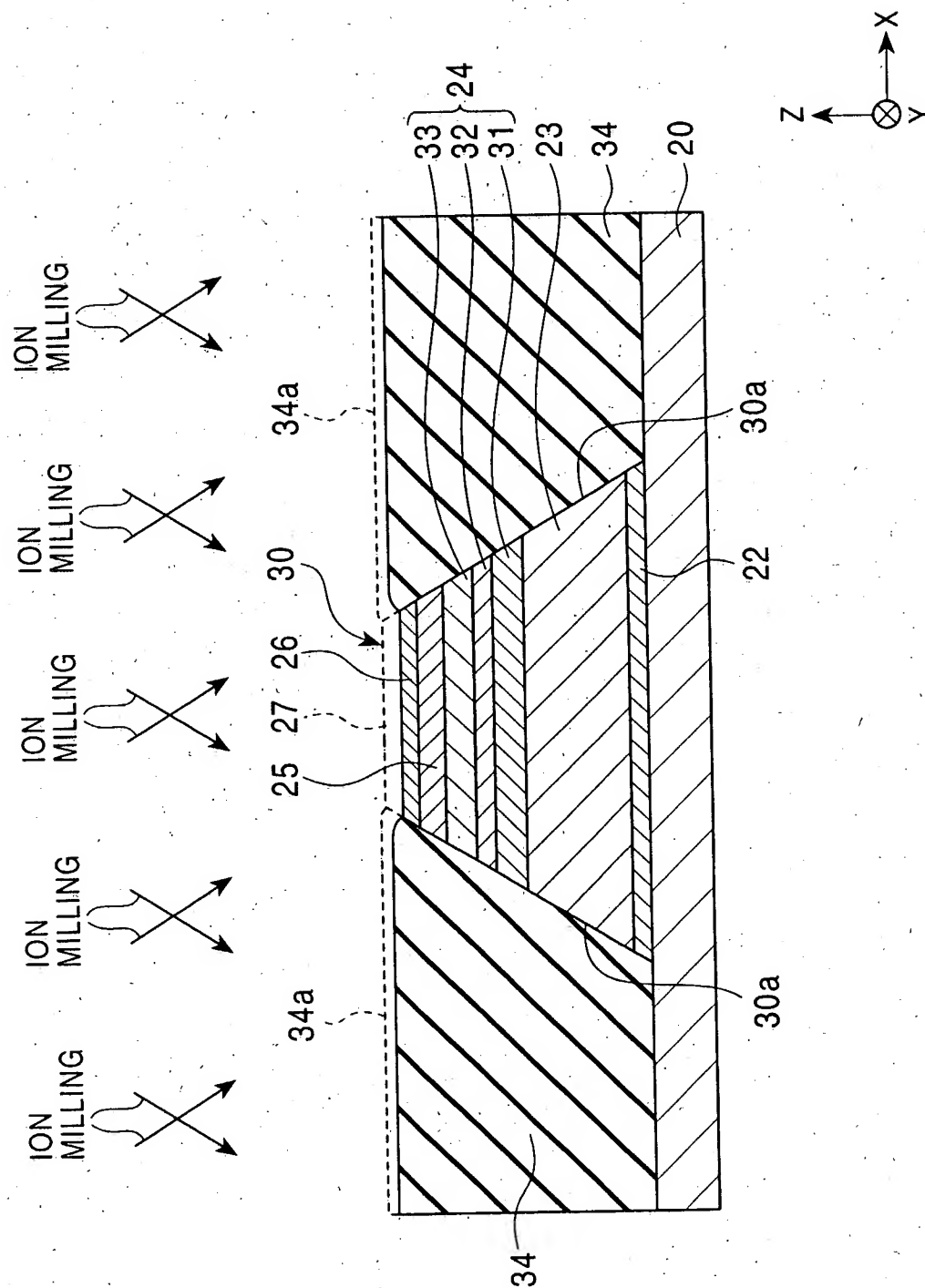


FIG. 8

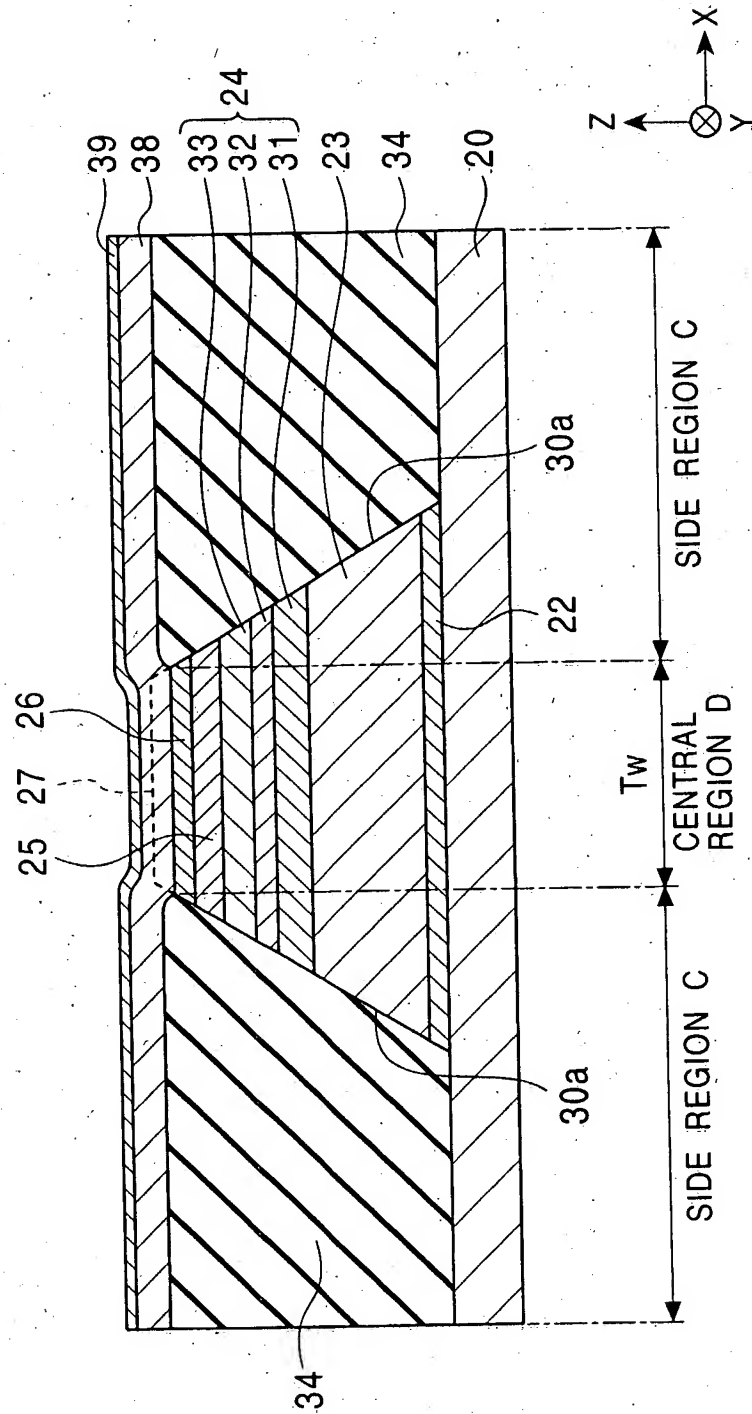


FIG. 9

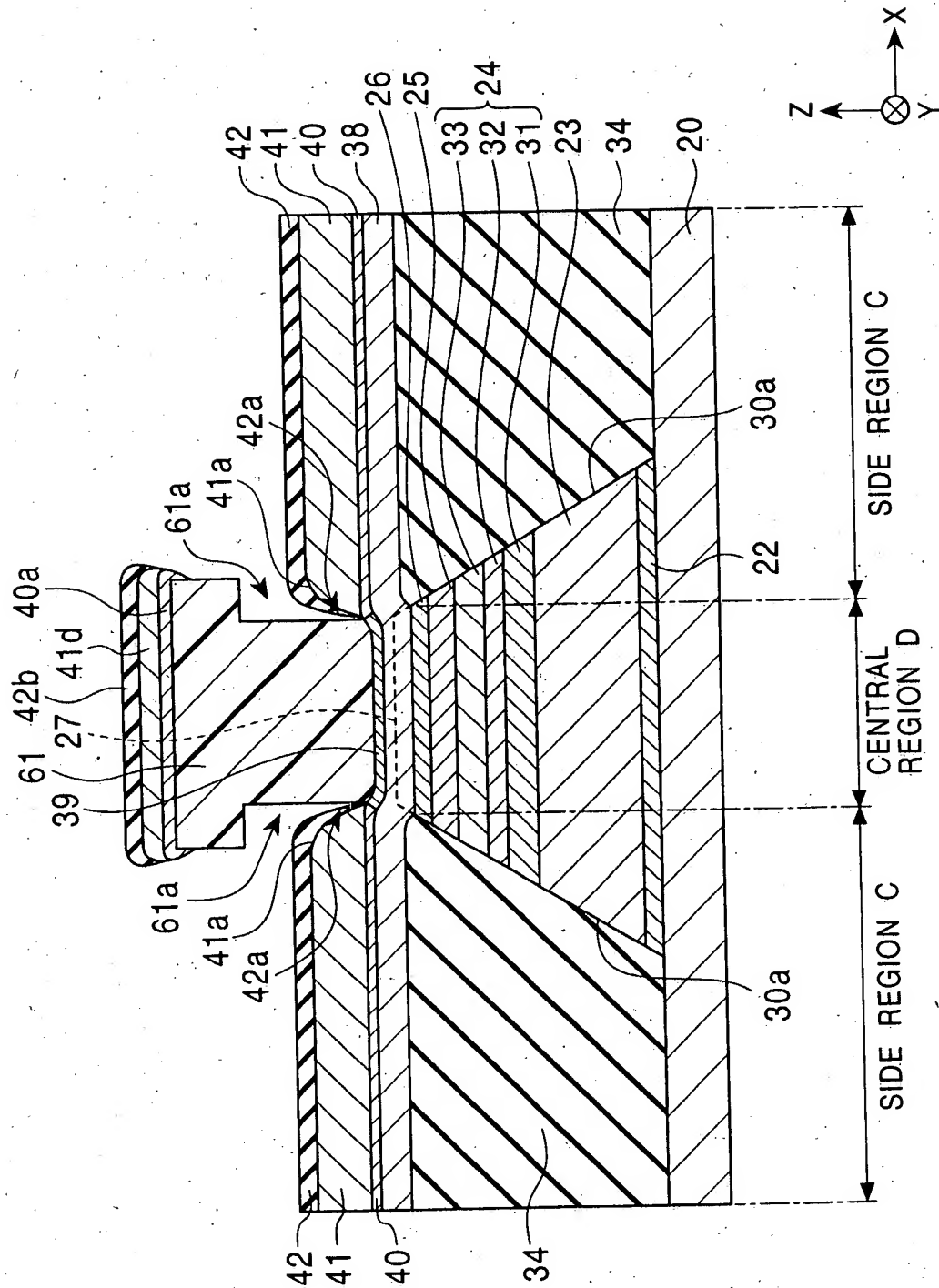
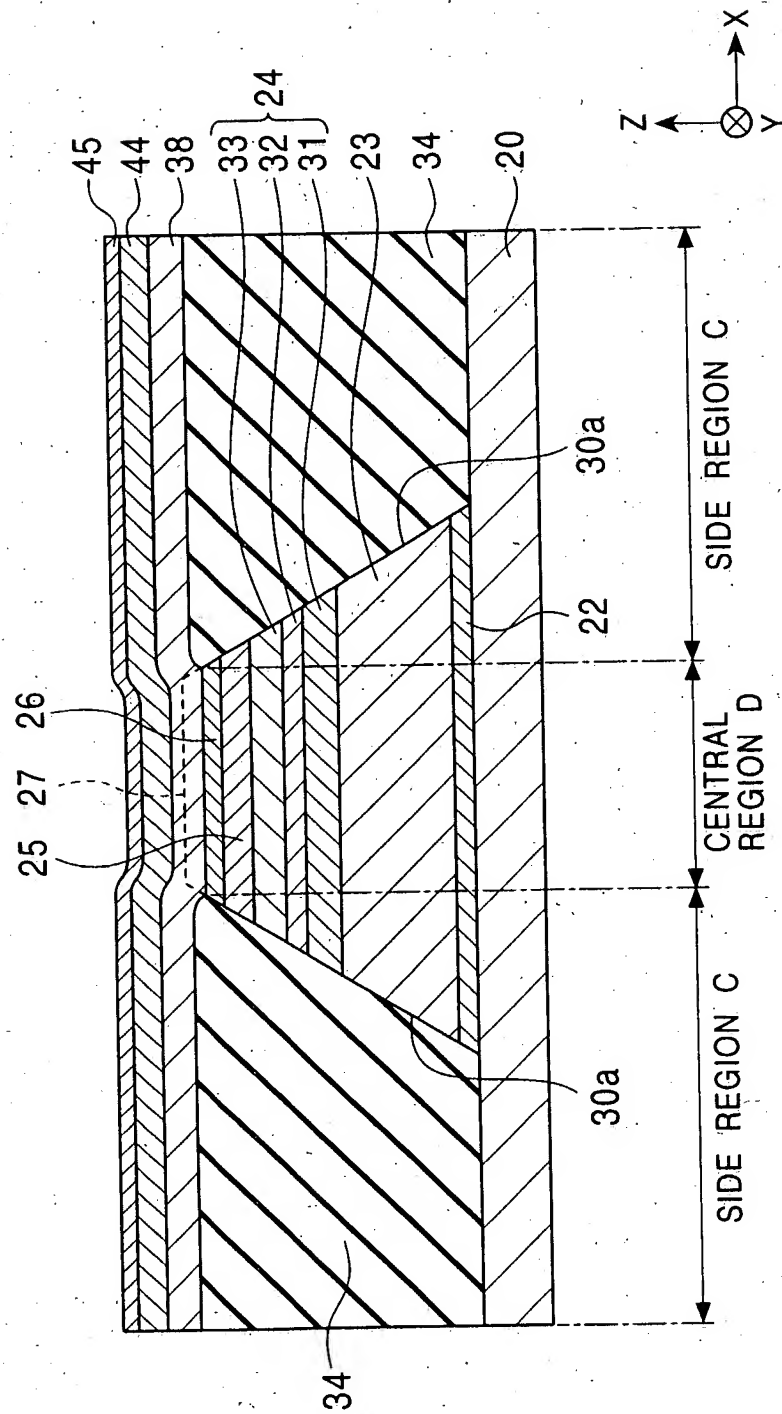


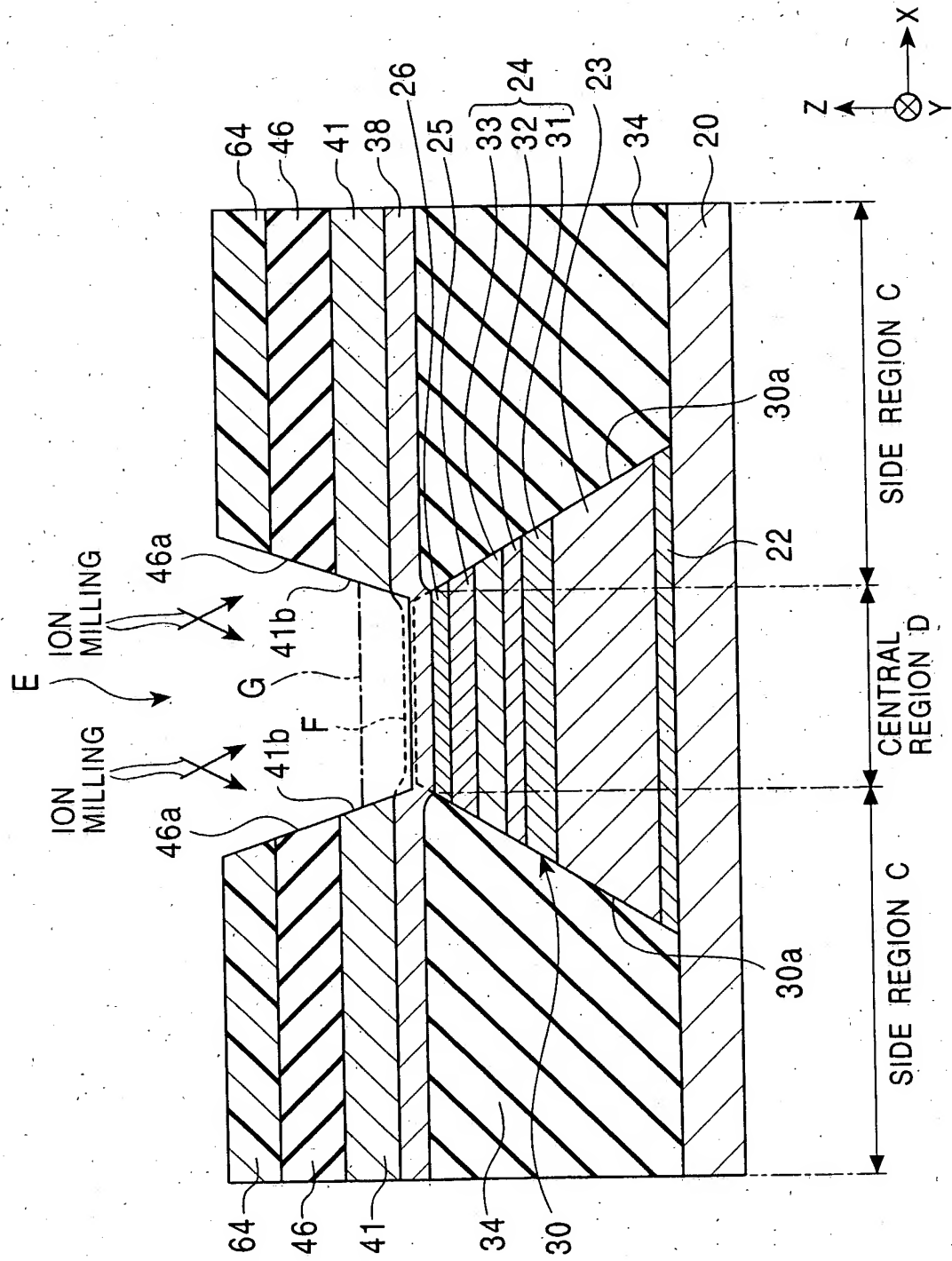
FIG. 10



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FIG. 13



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FIG. 14
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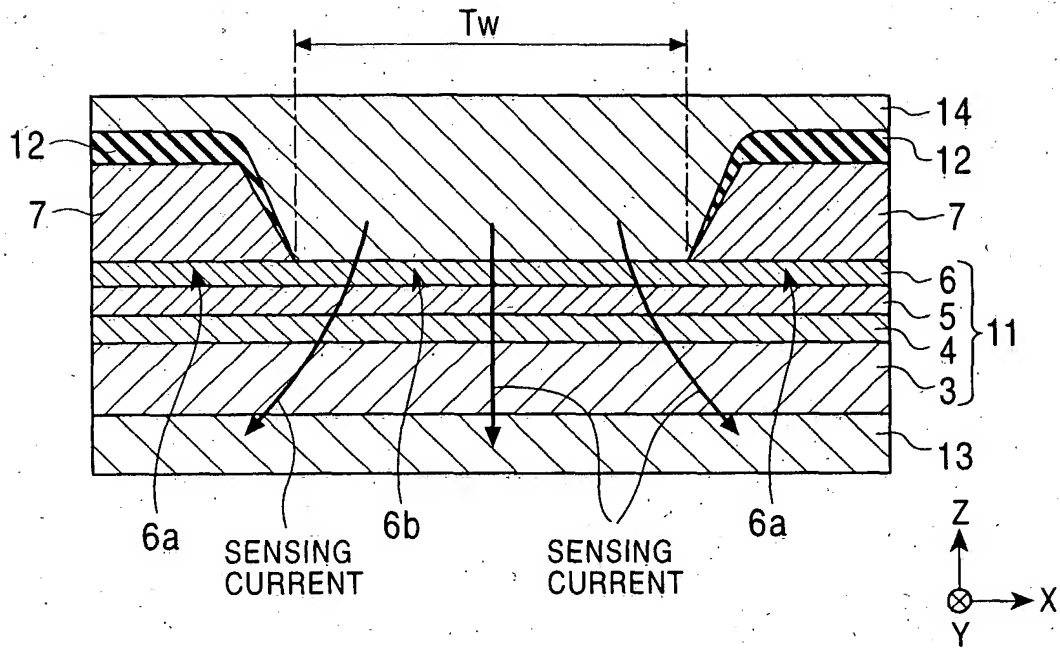


FIG. 15
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